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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/624,398 | 07/22/2003 | Leo Mathew | SC12862TC | 6797 |

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| EXAMINER | |
|---|---|
| SIEK, VUTHE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

N·A

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/624,398 | MATHEW ET AL. | |
| | Examiner | Art Unit | |
| | Vuthe Siek | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,12-14,19 and 20* is/are rejected.

7)☒ Claim(s) *5-11 and 15-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to application 10/624,398 filed on 7/22/2003. Claims 1-20 remain pending in the application.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. According to the specification, a first intermediate layer 18 and second intermediate layer 20 are created and with the "AND" operation layer 22 is created to define spacing between at least two fins (see Fig. 5 and its description). Therefore claiming defining at least one intermediate layer to create a spacing is not descriptive. Suppose one intermediate layer is created (this meets claiming defining at least one intermediate layer), that one intermediate layer is not able to define a spacing between at least two fins.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Chan et al. (US 2004/0266115).

6. As to claims 1-2 and 19-20, Chan et al. teach a method of making a multiple gate transistor on a semiconductor device comprising a multiple fins (item 2), multiple gate electrode (item 3) over the fins and being a layer of gate electrode material with substantially planar surface (item 13b) to support a patterned mask (item 14a), where the mask having a uniform thickness and a planar surface controlling the patterning dimensions of the patterned mask (see Figs. 1-9). Figs. 4 and 5 show multiple fins are created within semiconductor layer (item 2a) on a planarized interlayer (item 5) of an insulator that covers an underlying substrate layer (item 4). The interlayer 5 comprises a dielectric or insulator. The fins are formed on the mask. The gate electrode material layer 13 tends to fill in the spaces between adjacent fins. Thus, Chan et al. teach making multiple gate transistor from planar transistor, where the multiple gate transistor has base planar transistor except for additional fins formed on the mask and where the fins having spaces filled with gate electrode material.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3-4 and 12-14 are rejected under 35 U.S.C. 103(a) as being obvious over Chan et al. (US 2004/0266115) in view of Tester (US 2004/0117748).

9. As to claim 13 and 3-4, Chan et al. teach a method of making a multiple gate transistor on a semiconductor device comprising a multiple fins (item 2), multiple gate electrode (item 3) over the fins and being a layer of gate electrode material with substantially planar surface (item 13b) to support a patterned mask (item 14a), where the mask having a uniform thickness and a planar surface controlling the patterning dimensions of the patterned mask (see Figs. 1-9). Figs. 4 and 5 show multiple fins are created within semiconductor layer (item 2a) on a planarized interlayer (item 5) of an insulator that covers an underlying substrate layer (item 4). The interlayer 5 comprises a dielectric or insulator. The fins are formed on the mask. The gate electrode material layer 13 tends to fill in the spaces between adjacent fins. Thus, Chan et al. teach making multiple gate transistor from planar transistor, where the multiple gate transistor has base planar transistor except for additional fins formed on the mask and where the fins having spaces filled with gate electrode material. Chan et al. do not teach using "AND" function to determine the overlapping region between the gate layer and the active layer and "XOR" functions to determine the resulting layer based on a non-overlapping region of the second intermediate layer and active layer. Tester teaches a method to create derivative integrated circuit layouts for a multiple products from a baseline product layout using a "XOR" function using layout software tools. It is noted

that "AND" function is inherently included with the layout software tools in order to performing an overlapping region between two layer regions. The baseline layout may be of an existing product (e.g. planar transistor). Additional layouts may be added to combine with the baseline layout in order to produce an objective layout product (e.g. multiple gate transistor by adding fins) (see Figs. 1-6 and its description). The fins are characteristic to define multiple gate transistor from the planar transistor. Accordingly, it would have obvious to one of ordinary skill in the art to use the layout software tools as taught by Tester in the process of making multiple gate transistor (Dual gate transistor) from the planar transistor as taught by Chan et al. because this would improve time to market for IC development since only additional layout (fins) are added to the planar transistor and the same changes don't need to be implemented several times in several products to thereby avoid costly iterations of designs because changes are not replicated.

10. As to claims 12 and 14, Chan et al. teach providing a semiconductor substrate and using the mask to create a semiconductor device overlying the semiconductor device, where the semiconductor device comprising a vertical double-gate transistor design (see summary, [0027-0033, 0039-0040].

***Allowable Subject Matter***

11. Claims 5-11 and 15-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach or

fairly suggest modifying a dimension of the first intermediate layer/oversizing the first intermediate, the second intermediate layer defines a length of the at least two fins to be greater than a length of the gate layer in the overlying region of the gate layer and the active layer.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER